AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-6. (Cancelled)

7. (previously presented) A serial communication device, comprising:

a central processing unit to execute a program;

a serial communication interface coupled to receive data from outside the serial communication device and to provide a transfer request signal and a timeout interrupt signal, the timeout interrupt signal being provided to the central processing unit when the data from outside the serial communication device is not received by the serial communication interface for a predetermined time;

a RAM including:

a buffer area to store the data, and

a work area for the program; and

a direct memory access controller coupled to receive the transfer request signal and to transfer the data from the serial communication interface to the buffer area, the direct memory access controller having set therein a first number as a number of transfers, the first number being

greater than a second number corresponding to a number of data received at a time by the serial communication interface,

wherein the direct memory access controller provides a data transfer end interrupt signal to the central processing unit when a transfer number of data received by the serial communication interface reaches the first number, and

wherein any data stored in the buffer area is transferred to the work area by the direct memory access controller when the central processing unit receives the data transfer end interrupt signal or the timeout interrupt signal.

8. (previously presented) A serial communication device according to claim 7,

wherein the serial communication interface includes a first-in first-out memory to store the data from outside the serial communication device, and

wherein the transfer request signal is provided to the direct memory access controller when a number of data received in the first-in first-out memory exceeds a number of data received trigger set in the serial communication interface.

9. (previously presented) A serial communication device according to claim 7,

wherein the direct memory access controller is started up before the serial communication interface receives the data from outside the serial communication device, and

wherein the first number is set in the direct memory access controller before the serial communication interface receives the data.

10. (previously presented) A serial communication device according to claim 9, wherein the serial communication interface further includes means for stopping the generation of data to be received by the serial communication interface from outside the serial communication device after the timeout interrupt signal has been generated.

11. (previously presented) A serial communication device comprising:

a central processing unit to execute a program;

a serial communication interface coupled to receive data from outside the serial communication device and to provide a transfer request signal, the serial communication interface including a timeout interrupt signal generation section to provide a timeout interrupt signal to the central

processing unit based on a timeout setting value for a period until the timeout interrupt signal is generated;

a memory including:

a buffer area to store the data, and

a work area for the program; and

a direct memory access controller coupled to receive the transfer request signal and to transfer the data from the serial communication interface to the buffer area, the direct memory access controller having set therein a first number as a number of transfers, the first number being greater than a second number corresponding to a number of data received at a time by the serial communication interface,

wherein the direct memory access controller provides a data transfer end interrupt signal to the central processing unit when a number of data transferred from the serial communication interface to the buffer area by the direct memory access controller reaches the first number, and

wherein any data stored in the buffer area is transferred to the work area by the direct memory access controller when the central processing unit receives one of the data transfer end interrupt signal and the timeout interrupt signal.

12. (currently amended) A serial communication device according to claim 11, wherein the timeout interrupt signal generation section includes:

a receive determination section coupled to receive the data from outside the serial communication device and to provide a count start trigger when the data is received;

a counter coupled to receive the count start trigger and to provide a count value; and

an overflow determination section coupled to receive the count value and the timeout setting value and to provide the timeout interrupt signal when the count value ~~is~~ exceeds the timeout setting value.

13. (previously presented) A serial communication device according to claim 12, wherein the timeout interrupt signal generation section further includes a register to store the timeout setting value.

14. (currently amended) A serial communication device according to claim 13, wherein the serial communication interface is configured to stop generation of the timeout interrupt signal until ~~the~~ next data is received by the serial communication interface, after the timeout interrupt signal has been provided.

15. (previously presented) A serial communication device according to claim 11,

wherein the serial communication interface includes a first-in first-out memory to store the data from outside the serial communication device, and

wherein the transfer request signal is provided to the direct memory access controller when a number of data received in the first-in first-out memory exceeds a number of data received trigger set in the serial communication interface.

16. (previously presented) A serial communication device according to claim 11,

wherein the direct memory access controller is started up before the serial communication interface receives the data from outside the serial communication device, and

wherein the first number is set in the direct memory access controller before the serial communication interface receives the data.

17. (previously presented) A serial communication device comprising:

a central processing unit to execute a program;

a serial communication interface coupled to receive data from outside the serial communication device and to

provide a transfer request signal, the serial communication interface including a timeout interrupt signal generation section to provide a timeout interrupt signal to the central processing unit based on a timeout value for a time period until the timeout interrupt signal is generated;

a memory including:

a first buffer area,

a second buffer area, and

a work area for the program; and

a direct memory access controller having a continuous transfer function and coupled to receive the transfer request signal and to transfer the data from the serial communication interface to one of the first buffer area and the second buffer area, the direct memory access controller providing a data transfer end interrupt signal to the central processing unit and changing a destination of a data transfer to the other of the first buffer area and the second buffer area,

wherein any data stored in the one of the first buffer area and the second buffer area is transferred to the work area by the direct memory access controller when the central processing unit receives one of the data transfer end interrupt signal and the timeout interrupt signal.

18. (previously presented) A serial communication device according to claim 17,

wherein the serial communication interface includes a first-in first-out memory to store the data from outside the serial communication device, and

wherein the transfer request signal is provided to the direct memory access controller when a number of data received in the first-in first-out memory exceeds a number of data received trigger set in the serial communication interface.

19. (previously presented) A serial communication device according to claim 17,

wherein the direct memory access controller is started up before the serial communication interface receives the data from outside the serial communication device, and

wherein the first number is set in the direct memory access controller before the serial communication interface receives the data.

20. (currently amended) A serial communication device according to claim 17,

wherein the timeout interrupt signal generation section includes:

a receive determination section coupled to receive the data from outside the serial communication device and to provide a count start trigger when determining reception of the data by the serial communication interface;

a counter to provide a count value, the counter being responsive to the count start trigger starting the counter's ~~its~~ count up operation; and

an overflow determination section to compare the count value with the timeout setting value and to provide the timeout interrupt signal based on a result of the comparison being that the count value has exceeded the timeout setting value.

21. (previously presented) A serial communication device according to claim 20, wherein the timeout interrupt signal generation section further includes a register to store the timeout setting value.

22. (currently amended) A serial communication device according to claim 20,

wherein the direct memory access controller has a first channel and a second channel,

wherein one of the first channel and the second channel is used for data transfer from the serial communication unit to one of the first buffer area and the second buffer area,

while the other one of the first channel and the second channel is used for a data transfer from the other one of the first buffer area and the second buffer area to the work area.

23. (previously presented) A serial communication device according to claim 17, wherein the serial communication interface is configured to stop the generation of the timeout interrupt signal until the serial communication interface receives next data, after the timeout interrupt signal is provided.